REMARKS

Claims 98-135 are pending in this application. Claims 98-101, 107-123, and 127-134 are presently under consideration. Claims 102-106, 124-126, and 135 are withdrawn from consideration without prejudice or disclaimer. Claims 107-124 and 127-134 are allowed.

Claims 98-101 stand rejected under 35 U.S.C. 103(a) as unpatentable over Nozaki et al. (U.S. Patent No. 6,570,222) in view of Gonzalez et al. (U.S. Pub. No. 2001/0016378). This rejection is respectfully traversed.

Independent claim 98 recites "A method of forming an image sensor comprising the steps of: forming a pixel within a substrate; forming an isolation region adjacent to said pixel; and forming an isolation gate over said isolation region; wherein said isolation gate extends beyond said isolation region and over at least a portion of a connection region formed adjacent to said isolation region; and wherein said isolation gate and said isolation region isolate adjacent pixels." The remaining rejected claims depend from claim 98.

The Office Action cites Nozaki as teaching each of the above features, with the exception of citing Gonzalez as teaching an isolation gate extending beyond the isolation region. More particularly, the Office Action states:

> Nozaki does not disclose the wherein the isolation gate extending beyond the isolation region.
>
> Gonzalez et al. disclose a method of forming a semiconductor device where an active region (23) is formed adjacent to an isolation region (26); and forming an isolation gate (42) in a portion of the isolation region, wherein the isolation gate (42) extends beyond the isolation region (23) (Fig. 12; para. 24 & 30).
>
> Since Nozaki and Gonzalez et al. are both from the same field of endeavor, a method of forming a semiconductor device, the purpose disclosed by Gonzalez et al. would have been recognized in the pertinent art of Nozaki. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nozaki by he isolation

> gate extending beyond the isolation region as taught by Gonzalez et al. **to decrease the current leakage and improve transistor performance (para. 3, 4).**

Office Action, January 11, 2007, page 4 (emphasis added). Applicant respectfully submits that Gonzalez does not teach an isolation gate. Furthermore, even assuming *arguendo* that Gonzalez teaches an isolation gate extending beyond an isolation region, there is no motivation to make that proposed modification of Nozaki in view of Gonzalez.

Initially, Applicants note that the cited Figure 12 of Gonzalez illustrates an intermediary structure formed during the fabrication, i.e., as a processing step, of a field effect transistor (FET). Gonzalez, paras. 18-22. Furthermore, the cited motivation to modify Nozaki in view of Gonzalez, emphasized above, is taken from the background and summary discussions of Gonzalez's invention. The cited benefit of decreasing current leakage, therefore, is attributed to the completed invention of Gonzalez. The Office Action's implicit contention that this benefit is directed to the intermediary structure of Figure 12 is not supported by Gonzalez's disclosure.

As noted, Gonzalez does not teach an isolation gate. As shown in Figure 16, the component 42 cited as teaching an isolation gate is rather a horseshoe-shaped "conductive line 42" forming both a gate of an FET and a voltage divider. Gonzalez, paras. 30 and 37. The voltage divider includes first and second resistive elements, which respectively correspond to the p-n-p junctions formed by portions 72-74-76 and 76-78-80 of the conductive line 42. Gonzalez, para. 38. The voltage divider provides a bi-level threshold voltage for the FET, which in turn increases the ratio of Ion/Ioff to thereby reduce current leakage. Gonzalez, paras. 2 and 39-41.

Thus, in addition to incorrectly construing the conductive line 42 as an isolation gate, the Office Action also incorrectly attributes the extension of that conductive line 42, beyond the isolation region 26, to the reduction of current leakage achieved by the voltage divider construction. As the conductive line 42 does

not teach an isolation gate extending beyond an isolation region, as claimed, neither Nozaki nor Gonzalez (alone or in combination) teaches this feature of the claimed invention. Furthermore, as the cited motivation does not pertain to the proposed modification, but rather pertains to the voltage divider construction of the FET, there is no suggestion to make the proposed modification.

Accordingly, in view of the above remarks, Applicants respectfully request that this rejection be withdrawn. If the rejection is not withdrawn, then Applicants respectfully request the Examiner to address each of the above arguments in accord with MPEP § 707,07(f) ("Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.").

Applicants believe the pending application is in condition for allowance.

Dated: April 11, 2007

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Steven T. Dickey
Registration No.: 54,066
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant